**LAB NO 10**



**Fall 2024**

**CSE-304L Computer Organization and Architecture Lab**

Submitted by:

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Reg no**. : 22PWCSE2144**

ClassSection **: A**

Signature: \_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

**Dr. Amaad Khalil**

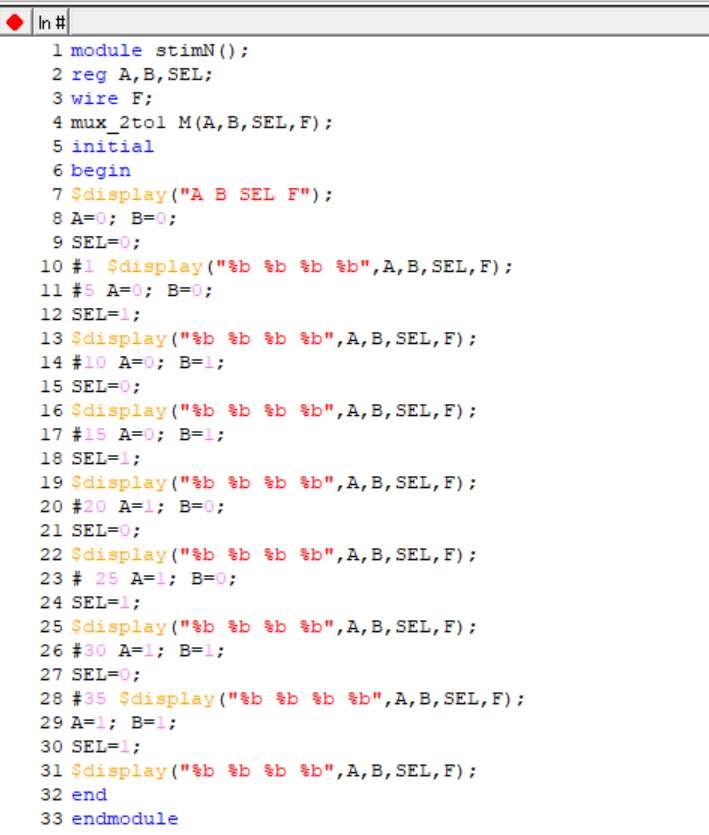
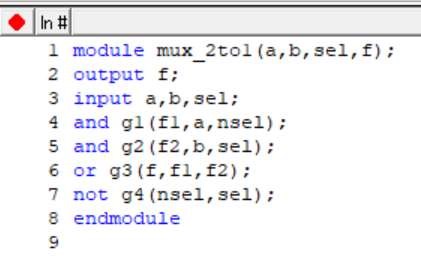
**Department of Computer Systems Engineering**

**University of Engineering and Technology, Peshawar**

# **MULTIPLEXER**

**TASK 01:**

**Write a Verilog code for 2x1 Mux using Dataflow Level modeling.**



A computer screen shot of a computer

Description automatically generated**Output:**

A screenshot of a computer

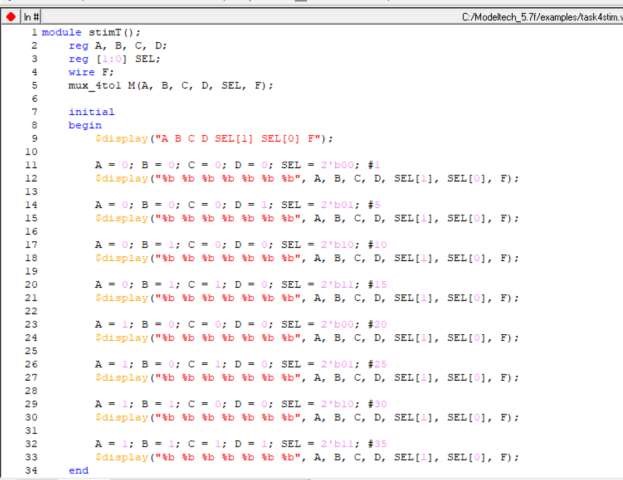
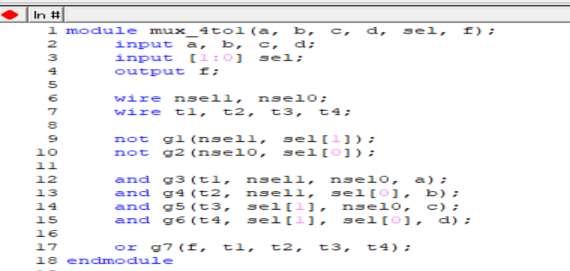
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A diagram of a circuit

Description automatically generated

**Task 02:**

**Write a Verilog code for 4x1 Mux using Dataflow Level modeling.**



**Output:**

**Table:**

A screenshot of a computer code

Description automatically generated

**Logical diagram:**

A diagram of a circuit

Description automatically generated

**Task3:**

**Write a Verilog code for 8x1 Mux using Dataflow Level modeling.**

A computer screen shot of a program

Description automatically generated

A screenshot of a computer program

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**Output:**

**Table:**

A screenshot of a computer

Description automatically generated